Ultra Low Power, Rail-to-Rail Output, Fully Differential Amplifier

Check for Samples: THS4531, THS4532

FEATURES

- **Ultra Low Power**
  - **Voltage: 2.5V to 5.5V**
  - **Current: 250μA/ch**
  - **Power Down mode 0.5μA (typ)**
- **Fully Differential Architecture**
- **Bandwidth: 35 MHz**
- **Slew Rate: 200 V/μs**
- **THD: –120dBc at 1kHz ($1V_{RMS}$, R_L=2kΩ)**
- **Input Voltage Noise: 10nV/rtHz (f=100 kHz)**
- **High DC Accuracy**
  - **V_{OS} < Drift ± 5μV/°C (max)**
  - **A_{OL} > 115dB**
- **RRO – Rail-to-Rail Output**
- **NRI – Negative Rail Input**
- **Output Common-Mode Control**

APPLICATIONS

- **Low Power SAR, ΔΣ ADC Driver**
- **Low Power, High Performance**
  - **Differential to Differential Amplifier**
  - **Single Ended to Differential Amplifier**
- **Low Power, Wide Bandwidth Differential Driver**
- **Low Power, Wide Bandwidth Differential Signal Conditioning**
- **High Channel Count and Power Dense Systems**

DESCRIPTION

The THS4531 family of devices is low power, fully differential op amps with input common-mode range below the negative rain and rail-to-rail output. They are designed for low power data acquisition systems and high density applications where power dissipation is critical.

The family includes single THS4531 and dual THS4532.

They feature accurate output common-mode control that allows for dc coupling when driving ADCs. This coupled with the input common-mode range below the negative rail and rail-to-rail output allows for easy interface between single ended ground referenced signal sources and SAR, and ΔΣ ADCs using only single supply 2.5V to 5V power supply.

The THS4531 family is characterized for operation over the extended industrial temperature range from –40°C to +125°C. The following package options are available:

- THS4531, 8 pin SOIC/VSSOP(MSOP) (D/DGK), 10 pin WQFN (RUN)
- THS4532, 16 pin TSSOP (PW)

PRODUCT PREVIEW

Table 1. Related Products

DEVICE	BW (MHz)	Iq (mA)	THD (dBc) at 100 kHz	VN(nV/√Hz)	RAIL-TO-RAIL
THS4521	145	1.14	-120	4.6	Out
THS4520	570	15.3	-114	2	Out
THS4121	100	16	–79	5.4	In/Out
THS4131	150	16	–107	1.3	No

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)

PRODUCT	CHANNEL COUNT	PACKAGE LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
THS4531	1	SOIC-8	D	–40°C to 125°C	TBD	THS4531ID	Rails, 75
	1				TBD	THS4531IDR	Tape and reel, 2500
	1	VSSOP-8	DGK	–40°C to 125°C	TBD	THS4531IDGKT	Tape and reel, 250
	1				TBD	THS4531IDGKR	Tape and reel, 2500
	1	WQFN-10	RUN	–40°C to 125°C	TBD	THS4531IRUNT	Tape and reel, 250
	1				TBD	THS4531IRUNR	Tape and reel, 2500
THS4532	2	TSSOP-16	PW	–40°C to 125°C	TBD	THS4532IPWT	Rails, 90
	2				TBD	THS4532IPWR	Tape and reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS

		VALUES	UNITS
Supply voltage, $V_{S–}$ to V_{S+}		5.5	
Input/Output Voltage, V_I ($V_{IN±}$, $V_{OUT±}$, V_{OCM} pins)		($V_{S–}$) – 0.7 to (V_{S+}) + 0.7	V
Differential input voltage, V_{ID}		1	V
Continuous output current, I_O		50	mA
Continuous input current, I_i		0.75	mA
Continuous power dissipation		See Thermal Characteristics Specification	
Maximum junction temperature, T_J		150	°C
Operating free-air temperature range, T_A		–40 to 125	°C
Storage temperature range, T_{stg}		–65 to 150	°C
ESD ratings:	HBM	3000	V
	CDM	500	V
	MM	200	V

THERMAL INFORMATION

THERMAL METRIC(1)		THS4531 SOIC (P) 8 PINS	THS4531 VSSOP (MSOP) (DGK) 8 PINS	THS4531 WQFN (RUN) 10 PINS	THS4532 TSSOP PW 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	144	269	146	TBD	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	84	75	75	TBD	
θ_{JB}	Junction-to-board thermal resistance	68	96	39	TBD	
ψ_{JT}	Junction-to-top characterization parameter	33	13	14	TBD	
ψ_{JB}	Junction-to-board characterization parameter	68	95	105	TBD	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

SPECIFICATIONS: V_S = 2.7 V

Test conditions unless otherwise noted: V_{S+} = 2.7 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2Vpp, R_F = 2kΩ, R_L = 2kΩ Differential, G = 1V/V, Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply, T_A = 25°C unless otherwise noted. **Blank specifications are TBD-delete when added.**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
AC PERFORMANCE						
Small-Signal Bandwidth	V_{OUT} = 100 mV_{pp}, G = 1		30		MHz	C
	V_{OUT} = 100 mV_{pp}, G = 2		13			
	V_{OUT} = 100 mV_{pp}, G = 5		4.5			
	V_{OUT} = 100 mV_{pp}, G = 10		3			
Gain-Bandwidth Product	V_{OUT} = 100 mV_{pp}, G = 10		30		MHz	
Large-Signal Bandwidth	V_{OUT} = 2 V_{pp}, G = 1		35		MHz	
Bandwidth for 0.1dB flatness	V_{OUT} = 2 V_{pp}, G = 1		20		MHz	
Slew Rate, Rise/Fall	V_{OUT} = 2 V Step		55/53		V/µs	
Rise/Fall Time			25/22		ns	
Settling Time to 1%, Rise/Fall			76/76		ns	
Settling Time to 0.1%, Rise/Fall			TBD			
Settling Time to 0.01%, Rise/Fall			TBD		ns	
Overshoot/UnderShoot, Rise/Fall			0.02/0.02%			
2nd Order Harmonic Distortion	f = 1 kHz, V_{OUT} = 1 V_{RMS}		–122		dBc	
	f = 10 kHz		–127			
	f = 1 MHz		–64			
3rd Order Harmonic Distortion	f = 1 kHz, V_{OUT} = 1 V_{RMS}		–130		dBc	
	f = 10 kHz		–135			
	f = 1 MHz		–69			
2nd Order Intermodulation Distortion	f = 1 MHz, 200 Hz Tone Spacing, V_{OUT} Envelope = 1V_{PP}		–81		dBc	
3rd Order Intermodulation Distortion			–78			
Input Voltage Noise	f = 100 kHz		10.25		nV/√Hz	
Voltage Noise 1/f corner frequency			TBD		Hz	
Input Current Noise	f = 1 MHz		0.5		pA/√Hz	
Current Noise 1/f corner frequency			TBD		kHz	
Overdrive recovery time, Over/Under	Overdrive = 0.5 V		TBD		ns	
Output Balance Error	V_{OUT} = 100 mV, f ≤ 10 kHz		–66		dB	
Closed-Loop Output Impedance	f = 1MHz (Differential)		TBD		Ω	
Channel to Channel Cross Talk (THS4532)	f = 10 kHz, measured differentially		TBD		dB	

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at 25°C; over temperature limits by characterization and simulation. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information.

PRODUCT PREVIEW

SPECIFICATIONS: V_S = 2.7 V

Test conditions unless otherwise noted: V_{S+} = 2.7 V, $V_{S–}$ = 0 V, V_{OCM} = open, V_{OUT} = 2Vpp, R_F = 2kΩ, R_L = 2kΩ Differential, G = 1V/V, Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply, T_A = 25°C unless otherwise noted. **Blank specifications are TBD.**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
DC PERFORMANCE						
Open-Loop Voltage Gain (A_{OL})		100	113		dB	A
Input Referred Offset Voltage	T_A = 25°C		±100		μV	A
	T_A = 0°C to 70°C					B
	T_A = –40°C to 85°C					
	T_A = –40°C to 125°C					
Input Offset Voltage Drift(2)	T_A = 0°C to 70°C		±2		μV/°C	B
	T_A = –40°C to 85°C					
	T_A = –40°C to 125°C					
Input Bias Current	T_A = 25°C		150		nA	A
	T_A = 0°C to 70°C					B
	T_A = –40°C to 85°C					
	T_A = –40°C to 125°C					
Input Bias Current Drift(2)	TA = 0°C to 70°C		±0.30		nA/°C	B
	T_A = –40°C to 85°C					
	T_A = –40°C to 125°C					
Input Offset Current	T_A = 25°C		±30		nA	A
	T_A = 0°C to 70°C					B
	T_A = –40°C to 85°C					
	T_A = –40°C to 125°C					
Input Offset Current Drift(2)	T_A = 0°C to 70°C		±60		pA/°C	B
	T_A = –40°C to 85°C					
	T_A = –40°C to 125°C					
INPUT						
Common-Mode Input Low	T_A = 25°C, < 3dB degradation in CMRR		$V_{S–}$ – 0.2	$V_{S–}$	V	A
	T_A = –40°C to 85°C, < 3 dB degradation in CMRR		$V_{S–}$ – 0.2	$V_{S–}$		B
Common-Mode Input High	T_A = 25°C, < 3dB degradation in CMRR	V_{S+} – 1.2	V_{S+} –1.1		V	A
	T_A = –40°C to 85°C, < 3 dB degradation in CMRR	V_{S+} – 1.2	V_{S+} –1.1			B
Common-Mode Rejection Ratio		100	116		dB	A
Input Impedance Common Mode			TBD		kΩ || pF	C
Input Impedance Differential Mode			TBD			C
OUTPUT						
Linear output voltage low	T_A = 25°C		$V_{S–}$ + 0.15	$V_{S–}$ + 0.2	V	A
	T_A = –40°C to 115°C		$V_{S–}$ + 0.15	$V_{S–}$ + 0.2		B
Linear output voltage high	T_A = 25°C	V_{S+} – 0.25	V_{S+} – 0.15		V	A
	T_A = –40°C to 115°C	V_{S+} – 0.25	V_{S+} – 0.15			B
Output saturation voltage, High / Low			80/40		mV	C
Linear output current drive	T_A = 25°C	±15	±22		mA	A
	T_A = –40°C to 115°C	±15				B
POWER SUPPLY						
Specified Operating Voltage		2.5		5.5	V	B
Quiescent Operating Current/ch	T_A = 25°C		230		μA	A
	T_A = –40°C to 85°C					B
Power Supply Rejection (±PSRR)		95	108		dB	A

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at 25°C; over temperature limits by characterization and simulation. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information.
(2) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.

PRODUCT PREVIEW

SPECIFICATIONS: V_S = 2.7 V (continued)

Test conditions unless otherwise noted: V_{S+} = 2.7 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2Vpp, R_F = 2kΩ, R_L = 2kΩ Differential, G = 1V/V, Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply, T_A = 25°C unless otherwise noted. **Blank specifications are TBD.**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
POWER DOWN						
Enable Voltage Threshold	Specified “on” above 2.1 V		1.3	2.1	V	A
Disable Voltage Threshold	Specified “off” below 0.7 V	0.7	1.3			A
Disable Pin Bias Current	$\overline{PD}$ = V_{S-} + 0.5 V		20		nA	A
Powerdown Quiescent Current	$\overline{PD}$ = V_{S-} + 0.5 V		0.5	1.5	µA	A
Turn-on Time Delay	Time from $\overline{PD}$ = high to V_{OUT} = 90% of final value		720		ns	C
Turn-off Time Delay	Time from $\overline{PD}$ = low to V_{OUT} = 10% of original value		110			
OUTPUT COMMON MODE VOLTAGE CONTROL (V_{OCM})						
Small-Signal Bandwidth	V_{OCM} = 100 mV_{PP}		25		MHz	C
Slew Rate	V_{OCM} = 1 V_{STEP}		15		V/µs	C
Gain			1		V/V	A
Common-Mode Offset Voltage			1		mV	A
Input Bias Current			0.9		nA	A
Output Common Mode Voltage Range		0.8	0.75 to 1.95	1.9	V	A
Input Impedance			165||0.86		kΩ || pF	C
Default Voltage offset from V_{S+}/2			2		mV	A

PRODUCT PREVIEW

SPECIFICATIONS: V_S = 5 V

Test conditions unless otherwise noted: V_{S+} = 5 V, $V_{S–}$ = 0 V, V_{OCM} = open, V_{OUT} = 2Vpp, R_F = 2kΩ, R_L = 2kΩ Differential, G = 1V/V, Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply, T_A = 25°C unless otherwise noted. **Blank specifications are TBD-delete when added.**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
AC PERFORMANCE						
Small-Signal Bandwidth	V_{OUT} = 100 mV_{pp}, G = 1		32		MHz	C
	V_{OUT} = 100 mV_{pp}, G = 2		14			
	V_{OUT} = 100 mV_{pp}, G = 5		5			
	V_{OUT} = 100 mV_{pp}, G = 10		3			
Gain-Bandwidth Product	V_{OUT} = 100 mV_{pp}, G = 10		30		MHz	
Large-Signal Bandwidth	V_{OUT} = 2 V_{pp}, G = 1		50		MHz	
Bandwidth for 0.1dB flatness	V_{OUT} = 2 V_{pp}, G = 1		30		MHz	
Slew Rate, Rise/Fall	V_{OUT} = 2 V_{Step}		200/290		V/µs	
Rise/Fall Time			5/5		ns	
Settling Time to 1%, Rise/Fall			8.7/5.7		ns	
Settling Time to 0.1%, Rise/Fall					ns	
Settling Time to 0.01%, Rise/Fall					ns	
Overshoot/UnderShoot, Rise/Fall			1.6/2.4%			
2^{nd} Order Harmonic Distortion	f = 1 kHz, V_{OUT} = 1 V_{RMS}		–122		dBc	
	f = 10 kHz		–128			
	f = 1 MHz		–65			
3^{rd} Order Harmonic Distortion	f = 1 kHz, V_{OUT} = 1 V_{RMS}		–130		dBc	
	f = 10 kHz		–137			
	f = 1 MHz		–70			
2^{nd} Order Intermodulation Distortion	f = 1 MHz, 200 kHz Tone Spacing, V_{OUT} Envelope = $2V_{PP}$		–70		dBc	
3^{rd} Order Intermodulation Distortion			–80			
Input Voltage Noise	f = 100 kHz		10		nV/√Hz	
Voltage Noise 1/f corner frequency			TBD		Hz	
Input Current Noise	f = 1 MHz		0.5		pA/√Hz	
Current Noise 1/f corner frequency			TBD		Hz	
Overdrive recovery time, Over/Under	Overdrive = 0.5 V		110		ns	
Output Balance Error	V_{OUT} = 100 mV, f = 100 MHz		–67		dB	
Closed-Loop Output Impedance	f = 1MHz (Differential)		TBD		Ω	
Channel to Channel Cross Talk (THS4542)	f = 10 kHz, measured differentially		–TBD		dB	

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at 25°C; over temperature limits by characterization and simulation. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information.

PRODUCT PREVIEW

SPECIFICATIONS: V_S = 5 V

Test conditions unless otherwise noted: V_{S+} = 5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2Vpp, R_F = 2kΩ, R_L = 2kΩ Differential, G = 1V/V, Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply, T_A = 25°C unless otherwise noted. **Blank specifications are TBD-delete when added.**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
DC PERFORMANCE						
Open-Loop Voltage Gain (A_{OL})		100	114		dB	A
Input Referred Offset Voltage	T_A = 25°C		±100		μV	A
	T_A = 0°C to 70°C					B
	T_A = –40°C to 85°C					
	T_A = –40°C to 125°C					
Input Offset Voltage Drift(2)	T_A = 0°C to 70°C		±1		μV/°C	B
	T_A = –40°C to 85°C					
	T_A = –40°C to 125°C					
Input Bias Current	T_A = 25°C		160		μA	A
	T_A = 0°C to 70°C					B
	T_A = –40°C to 85°C					
	T_A = –40°C to 125°C					
Input Bias Current Drift(2)	TA = 0°C to 70°C		±0.30		nA/°C	B
	T_A = –40°C to 85°C					
	T_A = –40°C to 125°C					
Input Offset Current	T_A = 25°C		±30		nA	A
	T_A = 0°C to 70°C					B
	T_A = –40°C to 85°C					
	T_A = –40°C to 125°C					
Input Offset Current Drift(2)	T_A = 0°C to 70°C		±60		pA/°C	B
	T_A = –40°C to 85°C					
	T_A = –40°C to 125°C					
INPUT						
Common-Mode Input Low	T_A = 25°C, < 3dB degradation in CMRR		V_{S-} – 0.2	V_{S-}	V	A
	T_A = –40°C to 85°C, < 3 dB degradation in CMRR		V_{S-} – 0.2	V_{S-}		B
Common-Mode Input High	T_A = 25°C, < 3dB degradation in CMRR	V_{S+} – 1.2	V_{S+} –1.1		V	A
	T_A = –40°C to 85°C, < 3 dB degradation in CMRR	V_{S+} – 1.2	V_{S+} –1.1			B
Common-Mode Rejection Ratio		100	116		dB	A
Input Impedance Common Mode			TBD		kΩ || pF	C
Input Impedance Differential Mode			200||1			C
OUTPUT						
Linear output voltage low	T_A = 25°C		V_{S-} + 0.15	V_{S-} + 0.2	V	A
	T_A = –40°C to 115°C		V_{S-} + 0.15	V_{S-} + 0.2		B
Linear output voltage high	T_A = 25°C	V_{S+} – 0.25	V_{S+} – 0.15			A
	T_A = –40°C to 115°C	V_{S+} – 0.25	V_{S+} – 0.15			B
Output saturation voltage, High / Low			80/40		mV	C
Linear output current drive	T_A = 25°C	±15	±26		mA	A
	T_A = –40°C to 115°C	±15				B
POWER SUPPLY						
Specified Operating Voltage		2.5		5.5	V	B
Quiescent Operating Current/ch	T_A = 25°C		250		μA	A
	T_A = –40°C to 115°C					B
Power Supply Rejection (±PSRR)		95	108		dB	A

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at 25°C; over temperature limits by characterization and simulation. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information.
(2) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.

PRODUCT PREVIEW

SPECIFICATIONS: V_S = 5 V (continued)

Test conditions unless otherwise noted: V_{S+} = 5 V, $V_{S–}$ = 0 V, V_{OCM} = open, V_{OUT} = 2Vpp, R_F = 2kΩ, R_L = 2kΩ Differential, G = 1V/V, Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply, T_A = 25°C unless otherwise noted. **Blank specifications are TBD-delete when added.**

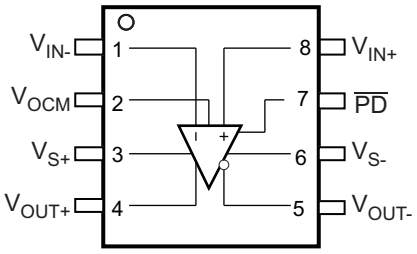
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
POWER DOWN						
Enable Voltage Threshold	Specified “on” above 2.1 V		1.3	2.1	V	A
Disable Voltage Threshold	Specified “off” below 0.7 V	0.7	1.3			A
Disable Pin Bias Current	$\overline{PD}$ = $V_{S–}$ + 0.5 V		20	500	nA	A
Powerdown Quiescent Current	$\overline{PD}$ = $V_{S–}$ + 0.5 V		0.5	1.5	µA	A
Turn-on Time Delay	Time from $\overline{PD}$ = high to V_{OUT} = 90% of final value		640		ns	C
Turn-off Time Delay	Time from$\overline{PD}$= low to V_{OUT} = 10% of original value		80			
OUTPUT COMMON MODE VOLTAGE CONTROL (V_{OCM})						
Small-Signal Bandwidth	V_{OCM} = 100 mV_{PP}		26		MHz	C
Slew Rate	V_{OCM} = 1 V_{STEP}		17		V/µs	C
Gain			1		V/V	A
Common-Mode Offset Voltage			1		mV	A
Input Bias Current			8		nA	A
Output Common Mode Voltage Range		0.8	0.75 to 4.2	4.15	V	A
Input Impedance			165||0.86		kΩ || pF	C
Default Voltage offset from V_{S+}/2			2		mV	A

PRODUCT PREVIEW

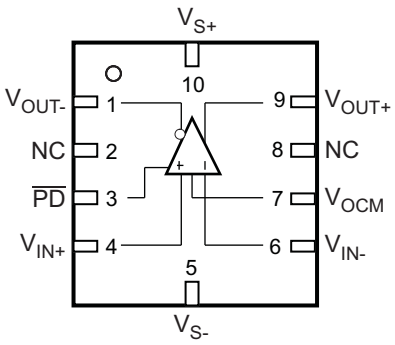
DEVICE INFORMATION

PIN CONFIGURATIONS

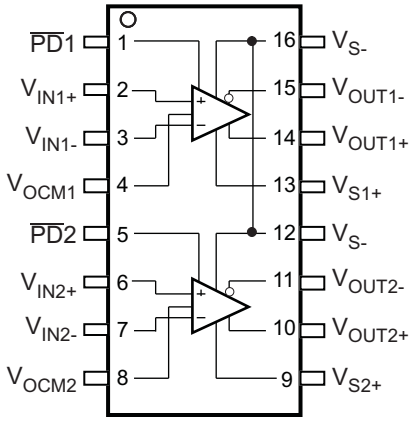
THS4531
SOIC-8 (D), VSSOP-8 (DGK) PACKAGE (TOP VIEW)



THS4531
WQFN-10 (RUN) PACKAGE (TOP VIEW)



THS4542
TSSOP-16 (PW) PACKAGE (TOP VIEW)



PRODUCT PREVIEW

PIN FUNCTIONS

NUMBER	NAME	DESCRIPTION
THS4531 D, DGK PACKAGE		
1	V_{IN-}	Inverted (negative) output feedback
2	V_{OCM}	Common-mode voltage input
3	V_{S+}	Amplifier positive power supply input
4	V_{OUT+}	Non-inverted amplifier output
5	V_{OUT-}	Inverted amplifier output
6	V_{S-}	Amplifier negative power supply input. Note V_{S-} tied together on multi-channel devices.
7	$\overline{PD}$	Powerdown, $\overline{PD}$ = logic low = low power mode, $\overline{PD}$= logic high = normal operation **(PIN MUST BE DRIVEN)**
8	V_{IN+}	Non-inverting amplifier input

PIN FUNCTIONS (continued)

NUMBER	NAME	DESCRIPTION
THS4531 RUN PACKAGE		
1	V_{OUT-}	Inverted amplifier output
2, 8	NC	No internal connection
3	$\overline{PD}$	Powerdown, $\overline{PD}$ = logic low = low power mode, $\overline{PD}$= logic high = normal operation **(PIN MUST BE DRIVEN)**
4	V_{IN+}	Non-inverting amplifier input
5	V_{S-}	Amplifier negative power supply input. Note V_{S-} tied together on multi-channel devices.
6	V_{IN-}	Inverting amplifier input
7	V_{OCM}	Common-mode voltage input
9	V_{OUT+}	Non-inverted amplifier output
10	V_{S+}	Amplifier positive power supply input
THS4532 PW PACKAGE		
1	$\overline{PD}_1$	Amplifier 1 powerdown, $\overline{PD}_1$ = logic low = low power mode amplifier 1, $\overline{PD}_1$ = logic high = normal operation amplifier 1 **(PIN MUST BE DRIVEN)**
2	V_{IN1+}	Amplifier 1 non-inverting input
3	V_{IN1-}	Amplifier 1 inverting input
4	V_{OCM1}	Amplifier 1 common-mode voltage input
5	$\overline{PD}_2$	Amplifier 1 powerdown, $\overline{PD}_2$ = logic low = low power mode amplifier 2, $\overline{PD}_2$ = logic high = normal operation amplifier 2 **(PIN MUST BE DRIVEN)**
6	V_{IN2+}	Amplifier 2 non-inverting input
7	V_{IN2-}	Amplifier 2 inverting input
8	V_{OCM2}	Amplifier 2 common-mode voltage input
9	V_{S2+}	Amplifier 2 positive power supply input
10	V_{OUT2+}	Amplifier 2 non-inverted (positive) output
11	V_{OUT2-}	Amplifier 2 inverted (negative) output
12	V_{S-}	Negative power supply input (common to both amplifiers)
13	V_{S1+}	Amplifier 1 positive power supply input
14	V_{OUT1+}	Amplifier 1 non-inverted (positive) output
15	V_{OUT1-}	Amplifier 1 inverted (negative) output
16	V_{S-}	Negative power supply input (common to both amplifiers)

TYPICAL CHARACTERISTICS: V_S = 2.7V

Test conditions unless otherwise noted: V_{S+} = 2.7 V, V_{S-} = 0V, CM = open, V_{OUT} = 2Vpp, R_F = 2kΩ, R_L = 2kΩ Differential, G = 1V/V, Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply unless otherwise noted.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS: V_S = 5V

Test conditions unless otherwise noted: V_{S+} = 5 V, $V_{S–}$ = 0V, V_{OCM} = open, V_{OUT} = 2Vpp, R_F = 2kΩ, R_L = 2kΩ Differential, G = 1V/V, Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply, T_A = 25°Cunless otherwise noted.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
THS4531ID	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
THS4531IDGK	PREVIEW	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
THS4531IDGKR	PREVIEW	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
THS4531IDR	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
THS4531IRUNR	PREVIEW	QFN	RUN	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
THS4531IRUNT	PREVIEW	QFN	RUN	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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